

Electrostatic Discharged Protection Devices (ESD) Data Sheet

Description

The UDS08A03L04 component is designed to protect low voltage state-of-the-art CMOS semiconductors from transients caused by electrostatic discharge (ESD), cable discharge events (CDE), lightning and other induced voltage surges. The device provides low stand-off voltages with significant reductions in leakage currents and capacitance over silicon avalanche diode processes.

The UDS08A03L04 features integrated low capacitance compensation diodes that reduce the typical capacitance 3pF per line.

This combined with low leakage current, means signal integrity preserved in high-speed applications such as 10/100/1000 Ethernet.

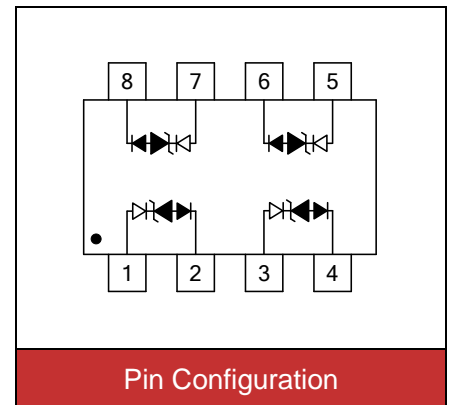


Contact : ±30kV
Air : ±30kV



Features

- IEC61000-4-2 ESD 30KV Air, 30KV contact compliance
- SOIC-08 surface mount package
- Protects four I/O lines
- Peak power dissipation of 400W under 8/20µs waveform
- Working voltage: 3.3V
- Low leakage current
- Low operating and clamping voltages
- Solid-state silicon avalanche technology
- Lead Free/RoHS compliant
- Solder reflow temperature: Pure Tin-Sn, 260~270°C
- Flammability rating UL 94V-0
- Meets MSL level 1, per J-STD-020
- Marking: B SLVU03-4



Applications

- 10/100/1000 Ethernet
- Instrumentation
- WAN/LAN Equipment
- Analog inputs
- High current switching systems
- Base stations
- Desktops, Servers and Notebook

Maximum Ratings

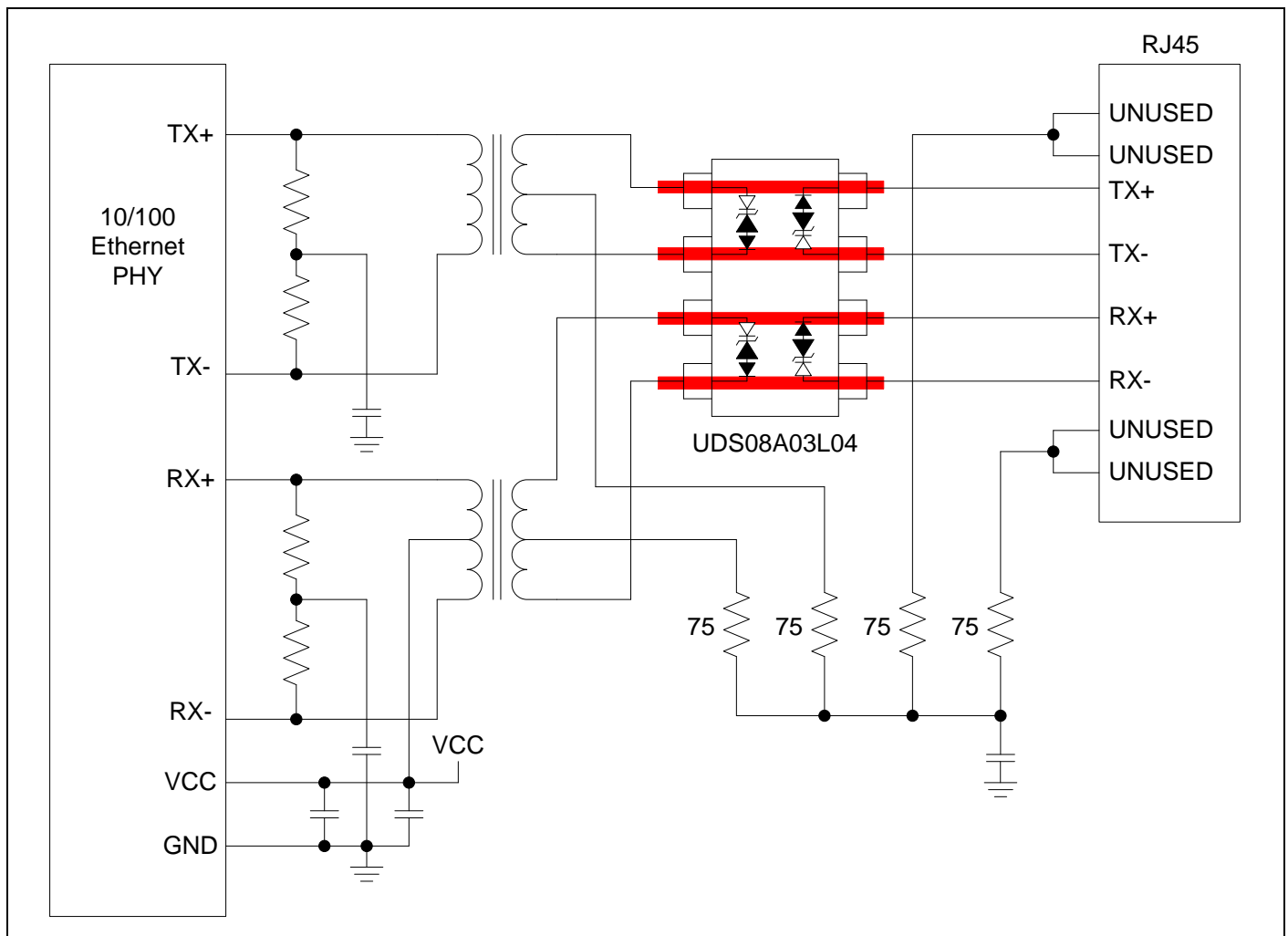
Rating	Symbol	Value	Unit
ESD voltage (Contact discharge)	V_{ESD}	±30	kV
ESD voltage (Air discharge)		±30	
Storage & operating temperature range	T_{STG}, T_J	-55~+150	°C

Electrical Characteristics ($T_J=25^{\circ}\text{C}$)

Parameter	Symbol	Condition	Min.	Max.	Unit
Reverse stand-off voltage	V_{RWM}			3.3	V
Reverse breakdown voltage	V_{BR}	$I_{BR}=1\text{mA}$	4.5		V
Reverse leakage current	I_R	$V_R=3.3\text{V}$ Each I/O pin		0.1	μA
Clamping voltage ($t_p=8/20\mu\text{s}$)	V_C	$I_{PP}=5\text{A}$		12.5	V
Peak pulse current ($t_p=8/20\mu\text{s}$)	I_{PP}			20	A
Off state junction capacitance	C_J	0Vdc, f=1MHz Between I/O pins and GND		1.5	pF
		0Vdc, f=1MHz Line to Line, two I/O pins connected together on each line (Note)		3	pF

Note: Ratings with two pins connected together per the recommended configuration (ie pin 1 connected to pin 8, pin 2 connected to pin 7, pin 3 connected to pin 6, pin 4 connected to pin 5).

Applications Information



Typical Characteristics Curves

Figure 1. Power Derating Curve

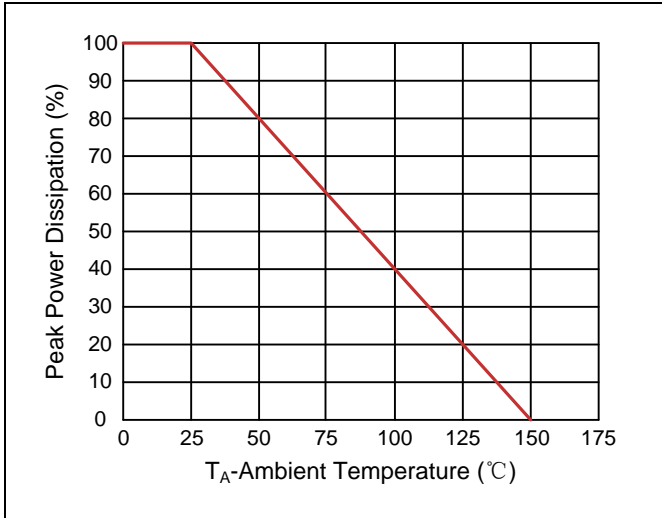


Figure 2. Pulse Waveforms

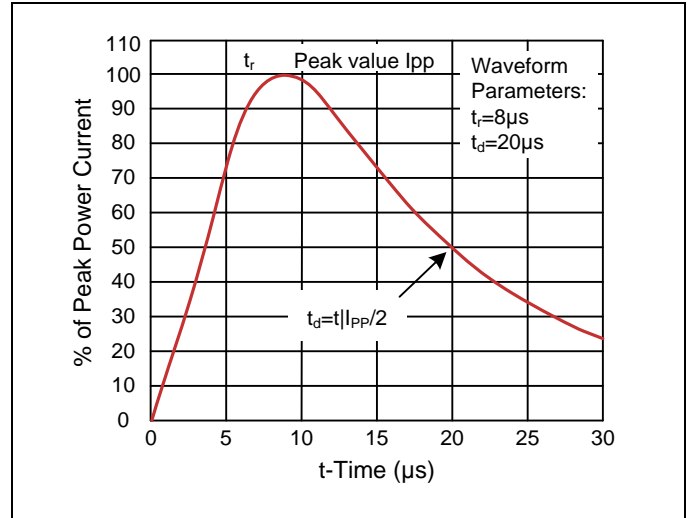


Figure 3. Non-Repetitive Peak Pulse vs. Pulse Time

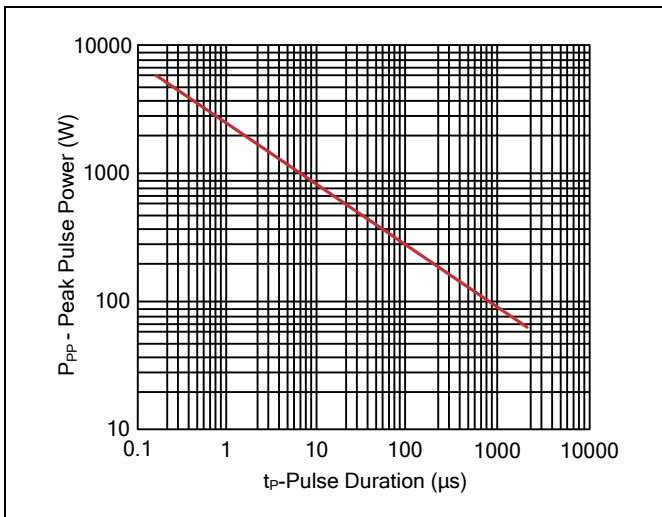


Figure 4. Capacitance vs. Reverse Voltage

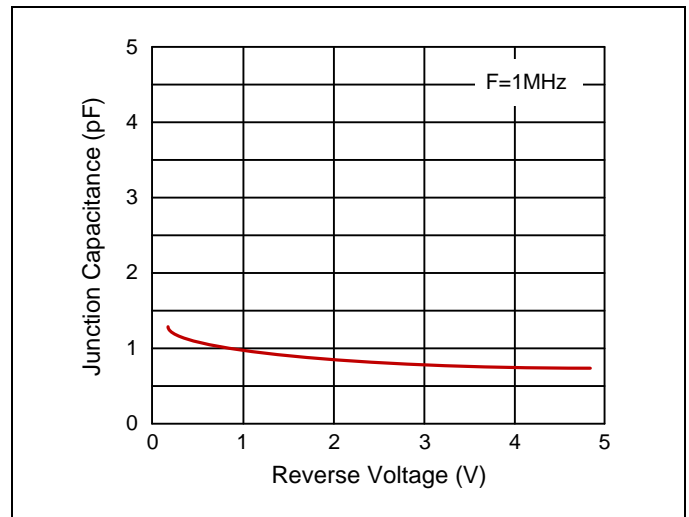
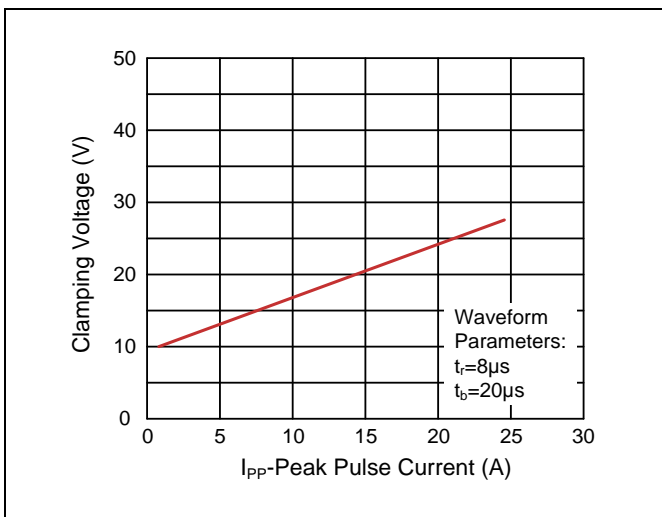
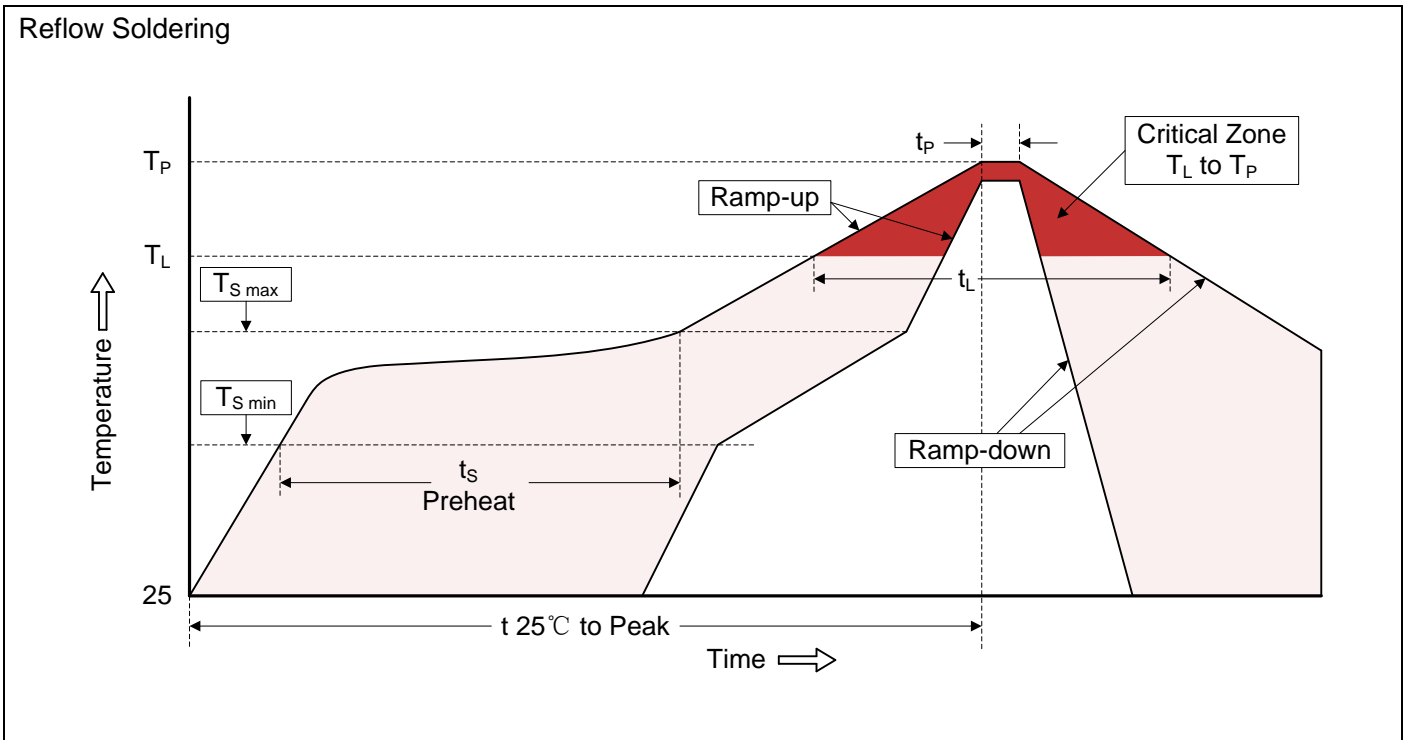


Figure 5. Clamping Voltage vs. Peak Pulse Current



Recommended Soldering Conditions



Recommended Conditions

Profile Feature	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.
Preheat -Temperature Min ($T_{S\ min}$) -Temperature Max ($T_{S\ max}$) -Time (min to max) (t_s)	150°C 200°C 60-180 seconds
$T_{S\ max}$ to T_L -Ramp-up Rate	3°C/second max.
Time maintained above: -Temperature (T_L) -Time (t_L)	217°C 60-150 seconds
Peak Temperature (T_P)	260°C
Time within 5°C of actual Peak Temperature (t_P)	20-40 seconds
Ramp-down Rate	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.

Dimensions (SOIC-08)

	Dimension				
	Symbol	Millimeters		Inches	
		Min.	Max.	Min.	Max.
	A	4.80	5.00	0.189	0.197
	B	5.80	6.20	0.228	0.244
C	3.80	4.00	0.150	0.157	
D	1.27		0.050		
E	0.33	0.51	0.013	0.020	
F	0.40	1.27	0.016	0.050	
G	0.19	0.25	0.007	0.010	
H	1.35	1.75	0.053	0.069	
H1	0.10	0.25	0.004	0.010	
H2	1.45		0.057		

Recommended Soldering Pad Layout

Packaging

<p>Tape</p>	Symbol	Dimension (mm)
	W	12.00±0.30
	P0	4.00±0.10
	P1	8.00±0.10
	P2	2.00±0.10
	D0	Φ1.55±0.10
	D1	Φ1.55±0.05
	E	1.75±0.10
	F	5.50±0.10
	A	6.50±0.10
	B	5.40±0.10
	K	2.00±0.10
	t	0.30±0.05

<p>Reel</p>	D	Φ330.0±3.0
	D2	Φ13.0
	W1	13.5
	Quantity: 2500PCS	